AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 2, line 25, and continuing to page 3 as follows:

If the clock in the receiving chip (e.g. the PHY) is slightly slower than that in the source (e.g. the MAC) there is significant danger that the 'elasticity buffer' will be overrun. Various expedients are available to avert this danger, on the assumption that the proximity of the danger can be detected. Those which involve discarding whole packets are unsuitable for high performance systems and those which rely on high and low watermarks of a FIFO tend to require large FIFO's and unnecessary complexity. It is also possible to discard preamble bytes but by itself this is an inappropriate solution, because some devices in the network may require the full complement of preamble bytes for correct operation.

Please amend the paragraph beginning at page 3, line 7, as follows:

A feature of the invention concerns the detection of small differences between clock frequencies employing an elasticity buffer ~~have~~having a write process controlled by one clock and a read process controlled by a second clock. According to one aspect of the invention a buffer having a minimal number, and more particularly five recycling storage locations is employed to detect small differences in clock rates and to generate a

A3 Cont.

resychronisation command, which may indicate a need to discard a byte (from a preamble or inter-packet gap).